A 60GHz 15.7mW Static Frequency Divider in 90nm CMOS

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***Abstract*—Two millimeter-wave current mode logic (CML) flip-flop-based static frequency dividers, divide-by-4 and by-2, are realized in a 90nm bulk CMOS. In order to achieve a large locking range and a high operating speed, capacitive-bridged shunt peaking techniques are implemented by taking advantage of the parasitic capacitance. The first flip-flop in these two dividers can directly drive the second flip-flop to save power, resulting in a power consumption as low as of 15.7mW from a 1.2V supply. Their input referred self-resonance frequencies are 57.6GHz and 61.4GHz respectively. Taking into account that all this is achieved in bulk CMOS, and even compared to SOI designs, the achieved power consumption is the lowest reported.**

I. INTRODUCTION

The frequency divider is one of the most critical components in a 60GHz phase-locked-loop (PLL), as it affects the PLL's power consumption, speed and locking range. To increase the operating frequency of a PLL, a dynamic frequency divider can be used, but its locking range is limited [1]. Therefore in this work a static frequency divider is used since it has a relatively wider locking range. Besides applications in PLL, the static divider is also an important block in high-speed digital circuits. Because the static divider is very sensitive to the technology speed, it is typically regarded as a technology benchmark to demonstrate the technology speed capability [2].

In the past, mm-wave static dividers were realized using SiGe or a compound technology [2]. With the improvement of device speed, several mm-wave CMOS static dividers have recently been reported [3]-[6]. To improve the speed of the static divider, a process modification and a circuit topology innovation should be explored [3], [4]. In [3]-[5], a modified 90nm or 65nm SOI process with pitch relaxation for low capacitance is used. In [5] and [6], inductor shunt peaking is used to increase the speed. In contrast to SOI, bulk CMOS has more capacitive parasitics, thus making it difficult to achieve high speed.

This paper presents two low power 90nm bulk CMOS static CML dividers: a divide-by-4 and a divide-by-2. To break the speed limit, a capacitive-bridged shunt peaking technique is employed by effectively using the routing parasitic capacitance. With this technique, the first flip-flop can directly drive the second one without using any buffer. So the DC power consumption is minimized while maintaining the center frequency at about 60GHz.

II. FREQUENCY DIVIDERS TOPOLOGY AND CIRCUIT DESIGN

As shown in Fig.1, the divide-by-4 circuit consists of a single-ended to differential converter (S2D), the first flip-flop (FF1), the second flip-flop (FF2) and two common-source amplifiers to drive the 50Ω measurement equipment. In the divide-by-2 circuit, the second flip-flop is omitted.

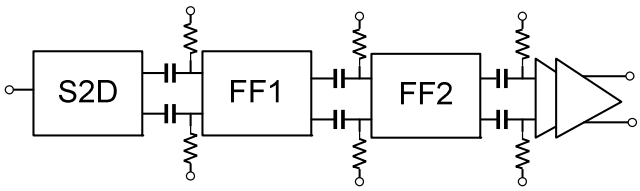

Figure 1. *The divide-by-4 circuit including single-ended to differential converter (S2D) and output buffers*

A. The divide-by-4 circuit

The divide-by-4 circuit is implemented by cascading two closed-loop CML flip-flop stages, in which the first flip-flop is shown in Fig. 2. Because the first flip-flop is the critical speed bottleneck, power hungry tapered buffers are typically inserted between flip-flops to reduce the capacitive load, leading to a speed advantage but a power penalty [6]. In this paper, these buffers are avoided by proper co-design and by using the proposed capacitive-bridged shunt peaking technique. Hence the first flip-flop can directly drive the second one, thereby saving a lot of DC power.

In the first flip-flop, the circuit speed is increased in three ways: (1) minimizing the delay time by reducing the

feedback line length; (2) increasing the transistor speed by biasing the transistor in high speed region using a high-pass capacitive-coupled level shifter. Also the tail current source is removed to save the voltage headroom for the speed; and (3) enhancing the rising and falling time by the capacitive-bridged shunt peaking technique. This technique will be explained next.

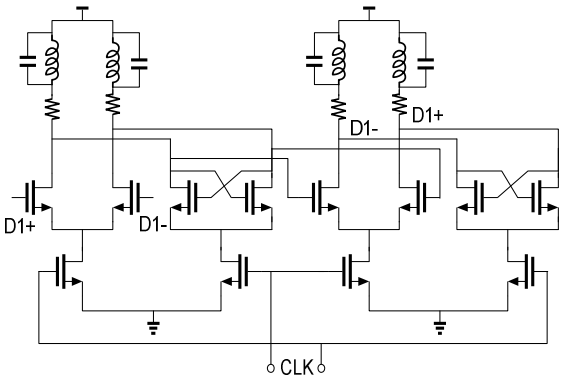

Figure 2. *The 1st flip-flop connected in closed-loop as a divider*

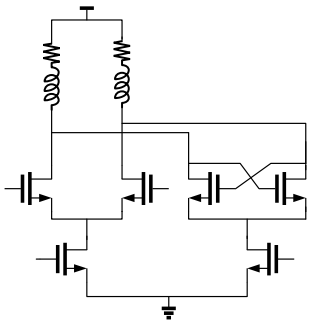

Figure 3. *The 1st flip-flop connected in closed-loop as a divider*

In the conventional shunt peaking [6], inductor and resistor is connected as shown in Fig.3. In this way, the inductor is connected directly to the drain side, the inductor parasitic capacitance to the ground cannot be distinguished from the drain capacitance. So the load capacitance C_L is increased. According to $L=mR^2C_L$, m≈ 0.3 [7], the inductor value has to be increased. As a result, the time constant RC_L also increases, reducing the speed. However, exchanging the position of the resistor and the inductor, as shown in Fig. 2, leads to the proposed capacitive-bridged shunt peaking, introducing more design freedom. In this way, the inductor parasitic capacitance to ground will be absorbed as a part of the bridged capacitance. This is also the case for the inter-winding capacitance. Compared with the conventional shunt peaking, simulations show that the capacitive-bridged shunt peaking technique has a 20% faster pulse settling and a 35% higher bandwidth. Therefore, with this technique, a lower power consumption and a higher speed can be achieved simultaneously.

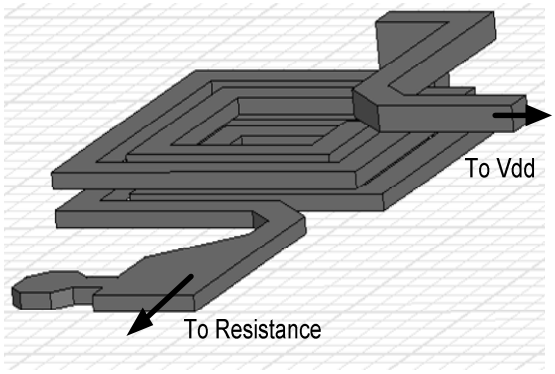

Figure 4. The 3D layout of the inductor used in the capacitive-bridged shunt peaking technique

In the capacitive-bridged shunt peaking technique, as the parasitic capacitance is absorbed in order to achieve a high speed, the inductor optimization strategy is different from the strategy in [8]. In [8], the inter-winding capacitance is reduced with the layer interleaving method. However this will increase the inductor area. With the proposed capacitive-bridged shunt peaking technique, for certain inductor value, the inductor area can be made much compact since more parasitic capacitance can be tolerated and used to maximized the speed with the proposed technique. In this paper, as shown in Fig.4, the realized inductor uses a three layer metal stack to reduce the area, and every metal layer has the same diameter. To achieve the required ratio between the bridged capacitance and the drain capacitance for the optimum transient performance, a small capacitance is realized using the bottom metal. In this design, the inductor is about 200pH and the resistor is about 70Ohm.

To save power, the second flip-flop is optimized to make its self-resonance frequency (*SRF*) half of the first. For improved common-mode rejection, a current source is added in the second flip-flop.

B. The divide-by-2 circuit

To make a comparison with other publication, a stand-alone divide-by-2 circuit is also realized. However, different from other publication, this divider drives a buffer which has the same capacitive loading as the second flip-flop to simulate a realistic loading.

C. The single-ended to Differential converter

For measurement purposes, a broadband single-ended to differential converter has been realized as shown in Fig. 5(a). Here the proposed peaking technique is used as well to reduce the rise time. At the input, a resistance and capacitance are connected in series, forming an AC termination resistance to avoid the signal reflection. Simulations show that the circuit insertion loss is about -12dB and the phase error is about 20 degree around 60GHz.

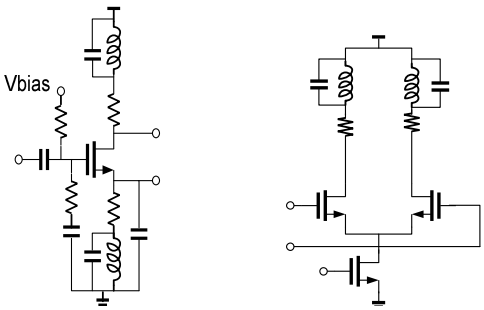

Figure 5. *The single-ended to differential converter (a) and buffer amplifier (b)*

D. Buffer amplifiers

For measurement purposes, two-stage buffer amplifiers have been realized only to drive the measurement equipment. Fig. 5(b) shows one stage buffer amplifier. As mentioned before, the transistor is sized to generate same loading capacitance as the flip-flop in the next stage.

III. MEASUREMENT RESULTS

A divide-by-2 and a divide-by-4 circuit were fabricated in a 90nm bulk CMOS. The die photos are shown in Fig. 6 and Fig. 7. The active area of these two dividers is about 68x80um2 and 150x80um2 respectively. With a 1.2V supply, the divide-by-2 consumes 15.7mW while the divide-by-4 consumes 21.8mW, of which 15.7mW for the first flip-flop and 6.1mW for the second flip-flop (the output buffer and the single-ended to differential converter power are excluded). A signal generator provides the test signal up to 67GHz. A spectrum analyzer is used to observe the output signal spectrum. Measurements of the divide-by-2 circuit show a locking range of 49GHz~67GHz with a center frequency of 61.4GHz. (as the input referred self-resonance frequency *ISRF* is equal to 2 times the output self-resonance frequency *OSRF,* which is 30.7GHz*)*. After de-embedding the loss of the cables and the single-ended to differential converter, the sensitivity curve is plotted in Fig. 8. The sensitivity curve of the divide-by-4 circuit is shown in Fig. 9. These curves show that the dividers indeed achieve a broad locking range with a limited power level. It shall be noted that this locking range is achieved under 20 degree phase error. Because the maximum locking frequency is limited by the input signal power level and phase error, a larger locking frequency range can be expected. In the divider-by-4 circuit, after powering down the first divider-by-2 stage, the *OSRF* of the second stage is measured. It is verified that the *OSRF* of the second stage is half of the first stage.

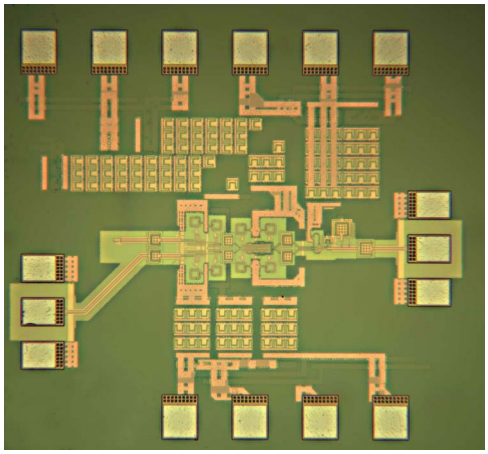

Figure 6. The die photo of the divide-by-2 circuit

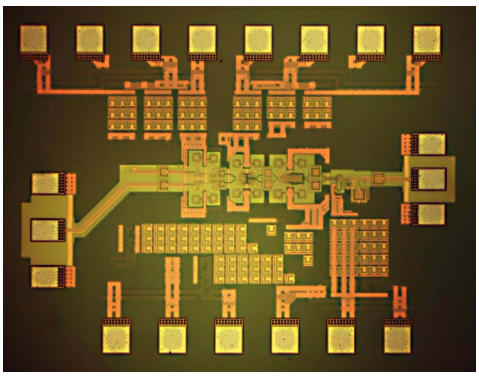

Figure 7. The die photo of the divide-by-4 circuit

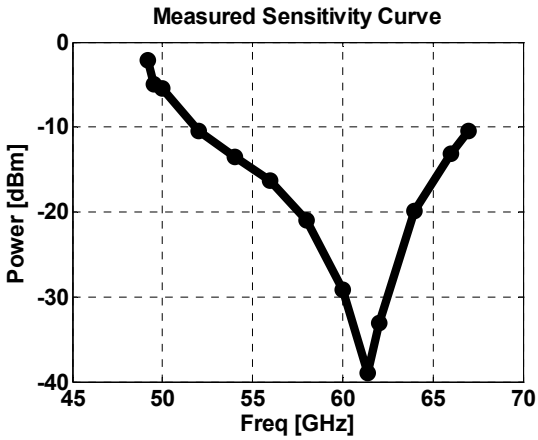

Figure 8. The measured sensitivity curve of the divide-by-2 circuit

TABLE I PERFORMANCE SUMMARY

FD	*ISRF* (GHz)	V_{dd} (V)	$Power_{DC}$ (mW)	*Divider Loading Info.*	*Tech.*	f_T (GHz)
Divide-by-2	61.4	1.2	15.7	Common Source Amp. (5mA 1st stage)	90 bulk	150
Divide-by-4	57.6	1.2	21.8 (15.7*)	Flip-Flop 2	90 bulk	150

(*power consumption of the first flip-flop)

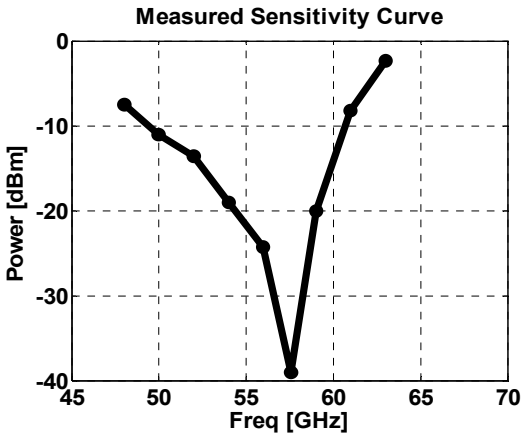

Figure 9. The measured sensitivity curve of the divide-by-4 circuit

In this paper, the presented dividers are realized using a 90nm bulk CMOS, with an f_T of 150GHz. Instead of using buffers between flip-flops, a high-pass capacitive-coupled level shifter is employed, resulting in even more power savings.

This can also be noticed if the power consumption of the first flip-flop, 15.7mW, is compared to [6], where the DC power consumption is 22.4mW. On top [6] is in a 65nm technology with a higher f_T of 195GHz. Even compared to those SOI designs [3-5], where the f_T is typically much higher, the power consumption of the proposed design is still the lowest of all. This is possible due to the speed advantage of the proposed capacitive-bridged shunt peaking technique, which was explained in section II.A.

A summary of the performance of the presented 60GHz dividers is given in Table I. Compared with the divide-by-2 circuit, the center frequency of the first flip-flop in the divide-by-4 circuit is a bit lower due to the longer interconnect lines. This emphasizes that the divider speed is very sensitive to the loading effect. Therefore, the table also gives the divider loading information.

In addition, it is noticed that [3]-[5] are standalone SOI divide-by-2 circuits, where they all use a source follower as buffer, where the loading capacitance is effectively reduced. Therefore, the power consumption of reported dividers can be reduced but with a higher power penalty of the source follower. Considering such issues, in our design, with the help of the proposed capacitive-bridged shunt peaking technique and high-pass capacitive-coupled level shifters, the first flip-flop can directly drive the second one, eliminating buffer stages to save DC power.

IV. CONCLUSION

By using the proposed capacitive-bridged shunt peaking technique, a bulk CMOS divide-by-2 and a divide-by-4 circuit are presented. The maximum speed is above 67GHz with a input referred self-resonance frequency of about 60GHz. The presented dividers achieve the lowest power consumption of 15.7mW at a 1.2V supply. The first flip-flop can directly drive the second one, avoiding buffer stages to save power.

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